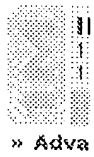


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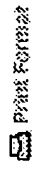
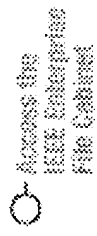
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1	X		US 20040107058 A1	20040603	51	Event pipeline and summing method and apparatus for event based test system	702/31
2	X		US 6532561 B1	20030311		Event based semiconductor test system	714/738
3	X		US 6226765 B1	20010501	14	Event based test system data memory compression	714/718
4	X		WO 2004008157 A2	20040122	76	EVENT PIPELINE AND SUMMING METHOD AND APPARATUS FOR EVENT BASED TEST SYSTEM	
5	X		WO 2004008157 A	20040122		Event pipeline and vernier summing apparatus for event based semiconductor test system, has pipelines incorporated in event vernier summing logic for processing event vernier data in parallel	

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1			Gomes, Glen et al.								US 20040107058	
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12	13388							
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